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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/871,596	05/30/2001	Noriyuki Saruhashi	81754.0061	8586

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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 10/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/871,596	SARUHASHI ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *4-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group I, claims 1-3 in Paper No. 5 is acknowledged.

Claims 4-13 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 5.

This application contains claims 4-13 drawn to an invention nonelected without traverse in Paper No. 5. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

Specification

2. The abstract of the disclosure is objected to because it includes references number to the drawings, the abstract should be rewritten in a manner that excludes any references to the drawings or specification. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 112

3. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. Claim 2 recites, "a test link layer circuit to be interrelated to said link layer interface". The omitted structural cooperative relationships are: the relationship between "a test link layer circuit" and "said link layer interface". Claim 2 recites, "a test physical layer logic circuit to be interrelated to said physical layer logic circuit". The omitted structural cooperative relationships are: the relationship between "a test physical layer logic circuit" and "said physical layer logic circuit".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 and 2 are rejected under 35 U.S.C. 102(e) as being anticipated by Shinozuka, Satoshi (US 6560200 B1).

35 U.S.C. 102(e) rejection of claim 1.

Shinozuka teaches a method for testing a physical layer device including a link layer interface, a physical layer logic circuit to be connected to said link layer interface (The circuit in Figure 1 of Shinozuka clearly provides a method for testing a physical layer device, Serial Bus Experimental Apparatus 2_n, including a link layer interface 5_n and a physical layer logic circuit 4_n connected to said link layer interface), and a plurality of ports to be connected to said physical layer logic circuit (Figure 6 in Shinozuka teaches that a plurality of ports are connected to any physical layer logic circuit 4_i through High Performance Serial Bus 1 and Serial Bus Cables 1_i), said method characterized in that: a test link layer circuit to be interrelated to said link layer interface (Packet Capture Circuit 32 in Figure 1 of Shinozuka is related to link layer interface 5_n, hence is a test link layer circuit) and a test physical layer logic circuit to be interrelated to said physical layer logic circuit (Packet Capture Circuit 32 in Figure 1 of Shinozuka is related to physical layer logic circuit 4_n, hence is a test physical layer logic circuit) are provided beforehand in said physical layer device(Packet Capture Circuit 32 in Figure 1 of Shinozuka is part of the physical layer device, Serial Bus Experimental Apparatus 2_n); in testing, said test link layer circuit (Packet Capture Circuit 32 in Figure 1 of Shinozuka) is connected to said physical layer logic circuit (physical layer logic circuit 4_n) through said link layer interface (link layer interface 5_n), and said test physical layer logic circuit (Packet Capture Circuit 32 in Figure 1 of Shinozuka) is connected to said physical layer logic circuit (physical layer logic circuit 4_n) through said plurality of ports (Note: Figure 6 in Shinozuka teaches that Packet Capture Circuit 32 in Figure 1 of Shinozuka is connected to physical layer logic circuit 4_i in Node Instrument 2_i through a plurality of

ports); and said link layer interface, said physical layer logic circuit, and said plurality of ports are tested (col.2, lines 14-30, Shinozuka).

35 U.S.C. 102(e) rejection of claim 2.

Shinozuka teaches a physical layer device with test circuits, said physical layer device including a link layer interface, a physical layer logic circuit to be connected to said link layer interface (Serial Bus Experimental Apparatus 2_n, includes a link layer interface 5_n, a physical layer logic circuit 4_n connected to said link layer interface, hence is a physical layer device with test circuits), and a plurality of ports to be connected to said physical layer logic circuit (Figure 6 in Shinozuka teaches that a plurality of ports are connected to any physical layer logic circuit 4_i through High Performance Serial Bus 1 and Serial Bus Cables 1_i), said physical layer device characterized by comprising: a test link layer circuit (Packet Capture Circuit 32 in Figure 1 of Shinozuka) for establishing, in testing, a connection with said physical layer logic circuit (physical layer logic circuit 4_n) through said link layer interface (link layer interface 5_n) and communicating predetermined data with said physical layer logic circuit (physical layer logic circuit 4_n); and a test physical layer logic circuit (Packet Capture Circuit 32 in Figure 1 of Shinozuka) for establishing, in testing, a connection with said physical layer logic circuit through said plurality of ports and communicating predetermined data with said physical layer logic circuit (Note during testing Note: Figure 6 in Shinozuka teaches that Packet Capture Circuit 32 in Figure 1 of Shinozuka is connected to physical layer logic circuit 4_i in Node Instrument 2_i through a plurality of ports).

35 U.S.C. 102(e) rejection of claim 3.

Each Node Instrument 2_i in Figure 6 has a control means for establishing a connection with an external link layer device or said test link layer circuit or for selectively establishing a connection with said physical layer logic circuit or said test physical layer logic circuit, hence the control means 3_i in Figure 6 are a switching means.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Vonbank, Michael et al. (US 6202103 B1) teaches data analyzers used to monitor bus traffic. Pugaczewski, John T. et al. (US 6069873 A) teaches systems used to test network and customer premise equipment (CPE) performance for compliance with appropriate protocol standards, and more particularly to improvements in test automation, monitoring, and recording for such a system. Paley, Daniel Noah et al. (US 6457152 B1) teaches testing protocol compliance of designs (such as Verilog designs) of a link layer for either the 1394-1995 or the 1394a bus protocols. Deguchi, Tomohiro et al. (US 6519544 B1) teaches a method and an apparatus for IEEE 1394 bus analysis used in product development of a 1394 bus interface circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-746-7240.

Joseph D. Torres, PhD
Art Unit 2133